**REMARKS**

After the foregoing amendment, claims 1-6 and 8-20 are active in the present application. Claim 10 has been amended to correct a grammatical error. No new matter has been added by the amendment. Entry of the Amendment is respectfully requested, as the Amendment places the application in condition for allowance.

Claims 1-20 stand rejected under 35 USC 103 as unpatentable over U.S. Patent Application No. 2004/0097081 (Igarashi) in view of U.S. Patent No. 5,568,363 (Kitahara). Igarashi forms the primary basis for the rejection and Kitahara is cited for teaching attaching a die to a bare metal sheet. Applicants respectfully traverse the rejection.

The present invention is directed to a method of packaging an integrated circuit die. A metal foil sheet has a single layer of solder formed on one side thereof. Subsequently, an IC die is attached to the solder layer. Die bond pods then are connected to the solder layer with a wire bonding process. In the wire bonding process, ball bonds are formed on the solder layer. The die and wire bonds are encapsulated and then the foil sheet is separated from the die and the wires. The package terminals comprise the ball bonds formed during the wire bonding process and a portion of the solder that remains attached to the ball bonds after the foil sheet is separated from the die.

Igarashi also teaches a method of packaging a semiconductor IC. However, instead of using a single layer of solder to form the package terminals, Igarashi teaches building the package with a patterned, multi-layer conductive laminate.

Igarashi forms a laminated plate 10 using first, second and third conductive films 11, 12 and 13. See Igarashi para. [0060]. A fourth conductive film 14 also is adhered to the plate 10. An etching process is performed to form pads 14A (Igarashi at [0068]). Additional complex and expensive etching steps are performed to remove portions of the films 11 and 13 (Igarashi at [0072] to [0079]).

In contrast, the present invention uses a single foil sheet with a layer of solder.

Igarashi FIG. 1 shows the formation of the multi-layer laminate. Compare to FIG. 2A of the present application, which shows a foil sheet and a single layer of solder.

Igarashi FIGS. 2-8 show the complex steps required to prepare the multi-layer laminate prior to attaching the IC die. The present invention does not require these complex processing steps.

Igarashi FIG. 9 shows an IC die attached to the multi-layered laminate, and bond wires attached to the multi-layered laminate. Compare Igarashi FIG. 9 to FIG. 2A of the present application, it can be seen that Igarashi teaches a multi-layered laminate (11A, 12, 13, 14A) and the present invention uses only a single layer of solder 32 formed on a foil sheet 30. So, not only is the IC attached to a multi-layered laminate 10, but the bond wires 20 are attached to the multi-layered laminate 10. In the present

invention, the bond wires 16 are attached directly to the single solder layer.

Igarashi FIG. 10 shows the die being encapsulated; which corresponds to FIG. 2C of the present application. FIG. 2C illustrates that the present invention includes a single layer of solder 32 to which the wires 16 are attached.

Igarashi FIG. 11 shows one of the conductive films 12 used to form the laminated plate 10 being removed; FIG. 2D of the present application, shows the foil sheet 30 and solder layer 32 being removed. Note that in the present application, the ball bonds are now exposed, whereas in Igarashi, the ball bonds are not exposed; rather the ball bonds are separated from the out side of the package by the layers 13, 11A and 14.

Igarashi FIG. 13 shows the steps of screen printing with solder cream and then reflow. In contrast, the present invention does not require such an additional step of screen printing solder cream because the package is formed using a layer of solder (32).

Finally, compare Igarashi FIG. 14 with FIG. 2E of the present application. Igarashi's final package has electrodes 24 that are connected to the IC bond pads not just via the wires 20, but also by way of the conductive layers 13, 11A and 14. FIG. 2E of the present application illustrates that the ball bonds of the bond wires 16 form the package terminals.

Kitahara is cited as disclosing a bare metal sheet, and the Office Action states that the bare metal sheet of Kitahara can be used in lieu of the multi-layered laminated plate 10 of Igarashi. Applicants respectfully disagree.

The metal sheet (3) of Kitahara is a lead frame. The present invention does not involve a lead frame. Rather, the present invention is method of forming a packaged device without using a lead frame.

Note that the leads (3) of Kitahara form an important part of the final package; whereas in the present invention, the foil sheet does not form any part of the final package. Rather, the "leads" of the present invention are the squashed ball bonds formed by the wire bonding and reflow processes. In the present invention, the foil sheet is removed. Thus, even combining Igarashi and Kitahara, a packaged device in which the package terminals are formed by the ball bonds of the wire bonding process is not provided.

At page 8, middle of the third paragraph, the Office Action avers that Igarashi discloses all of the limitations of claim 1 except for a foil sheet that comprises a bare metal sheet. Applicants respectfully disagree.

As discussed above, Igarashi discloses a very different method of forming a packaged device. Igarashi attaches the die to the laminated plate and attaches the wires to the laminated plate, and the laminated plate forms part of the final package.

In the present invention, the metal plate (foil sheet 10) does not form a part of the final package.

The Office Action also states that it would have been obvious to replace a layer of Igarashi with a foil sheet as taught by Kitahara for supporting the chip during process steps (Office Action, page 8, last sentence of third paragraph). However, Igarashi already has a layer, i.e., the second conductive layer 12, that provides mechanical

support (Igarashi at [0087]) and which subsequently is removed (See Igarashi FIG. 10 with layer 12 and FIG. 11 with layer 12 removed).

Each of the independent claims 1, 15 and 18 of the present invention recites the use of a foil sheet with a single layer of solder. The package terminals are formed by ball bonding to the solder layer, performing a reflow, and then removing the foil sheet. There is neither a lead frame nor a multi-layer substrate used in the process. The present invention is therefore very different from the processes taught by Igarashi and Kitahara, either alone or in combination. Accordingly, Applicants respectfully request that the rejection under section 103 be withdrawn.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application, including claims 1-6 and 8-20, is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

**Hei Ming SHIU *et al.***

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(Date)

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